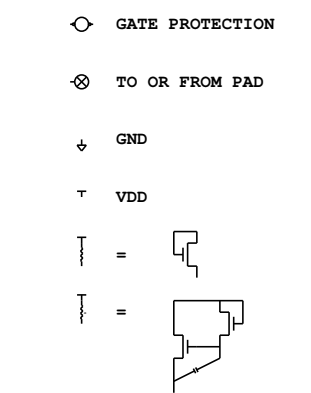


**4004 ADDRESS REGISTER
INCREMENTER AND INDEX REGISTER**

PIN CONFIGURATION

D0	1	16	CM RAM 0
D1	2	15	CM RAM1
D2	3	14	CM RAM2
D3	4	13	CM RAM3
GRND	5	12	VDD
CLK1	6	11	CM ROM
CLK2	7	10	TEST
SYNC	8	9	POC



Re-drawn schematic based on Revision G of the original Intel 4004 schematics by Intel Corporation (August 6, 1976). Schematic capture and design verification by Fred Rueftig, Brian Silveiman and Barry Silveiman (February 2, 2006).

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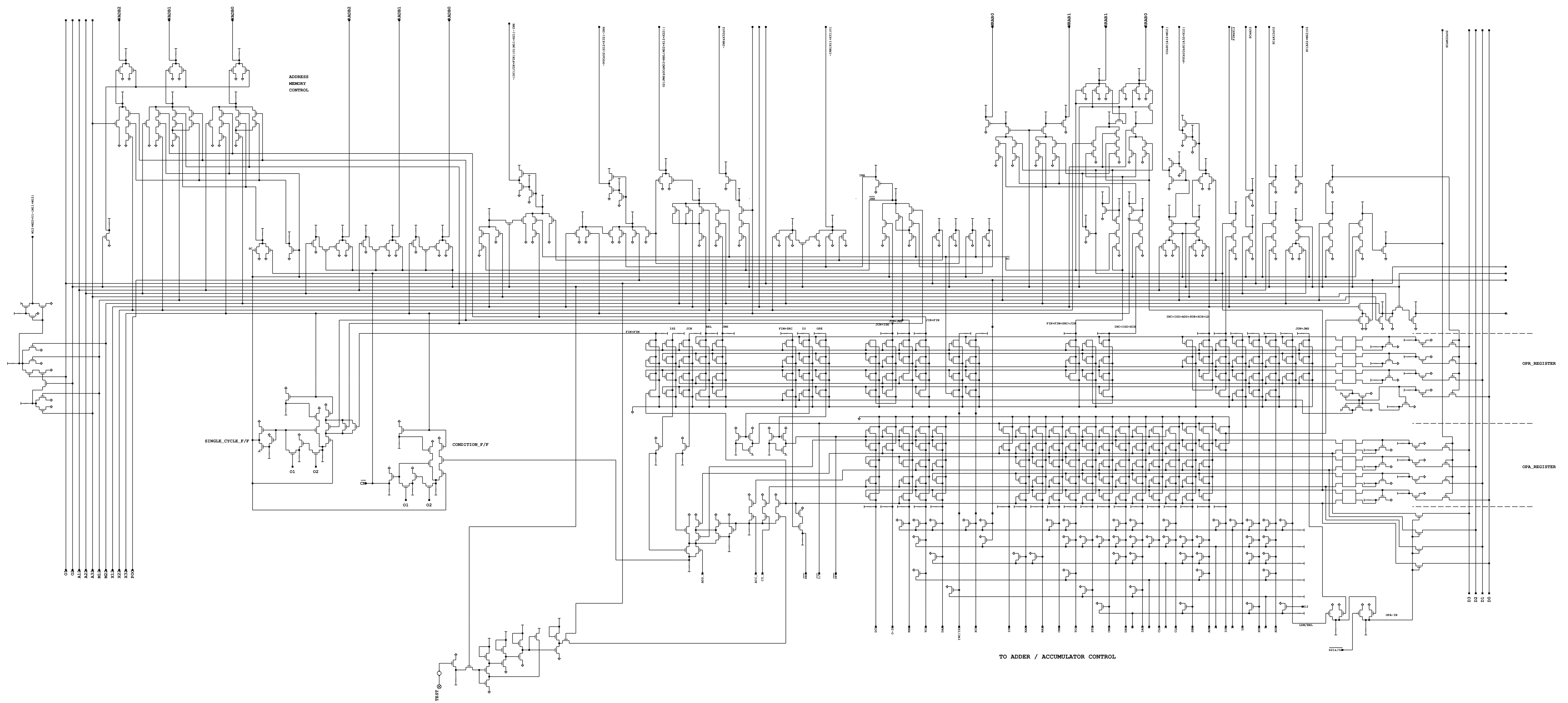
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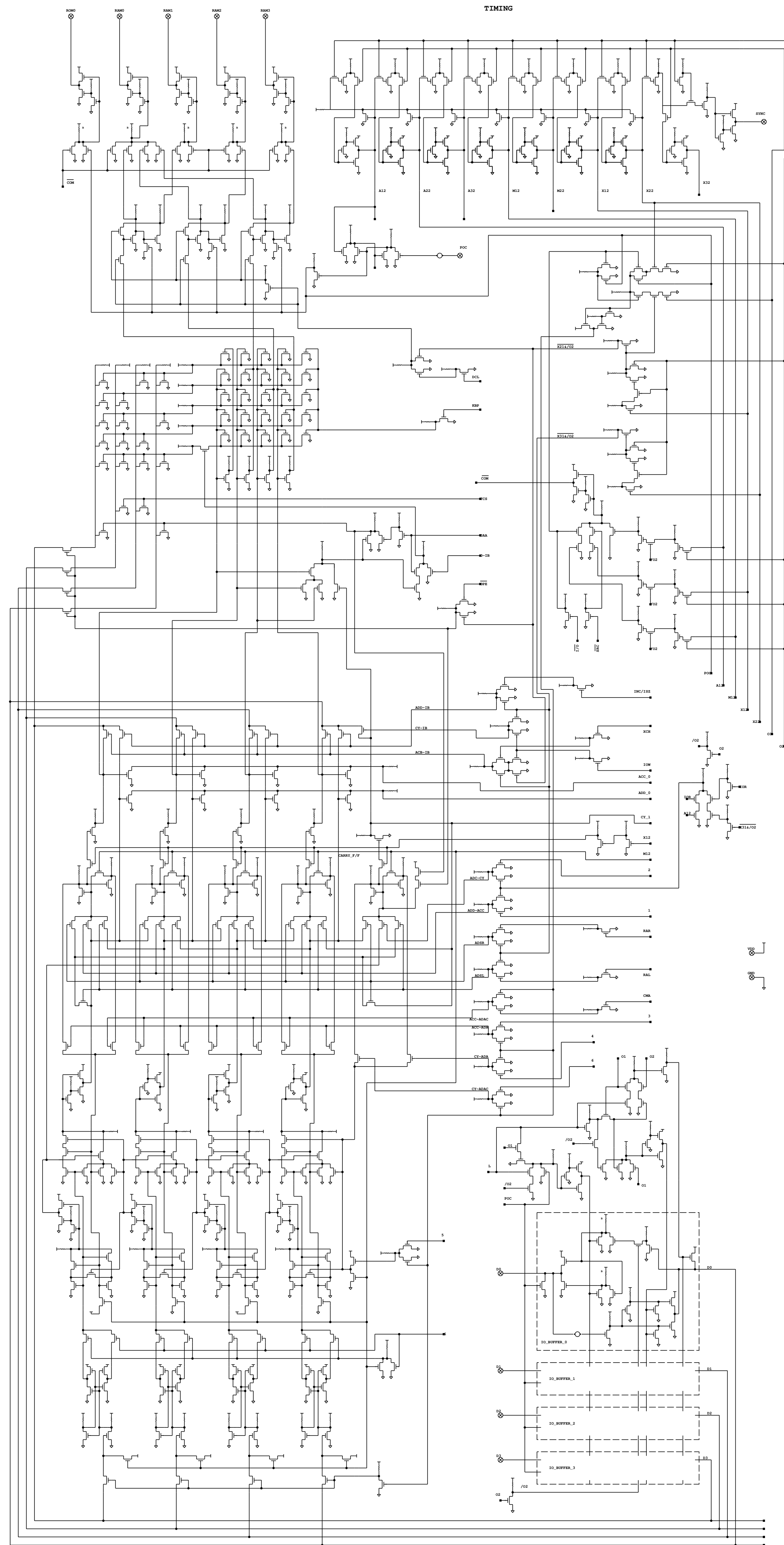
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